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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,292	07/12/2004	Carsten Deppe	DE020015	5664

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
TON, MY TRANG	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/501,292	DEPPE, CARSTEN	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 July 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER
9/21/05

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~7/21/04~~ 7/12/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (U.S Patent No. 5,543,740) cited in PTOL 1449.

Wong discloses in Figs. 1-2 an integrated half-bridge driver circuit including:

a driver circuit (Figs. 1-2) for controlling upper and lower switching means (14 and 16) for converting a direct voltage (18) into a clocked output voltage (22) for a resonant converter with a high-voltage section (40, 36, 32, 30, 42, 44, 46,) for controlling the upper switching means (14) and a low-voltage section (24, 28) for controlling the lower switching means (16) which switch the switching means (14, 16) on alternately, the switch-on phases of the switching means (14, 16) being separated from one another by dead-time phases, characterized in that there is provided a first circuit section (40, 30, 32, 72) which controls the duty cycle of the upper switching means (14) as a function of the duty cycle of the lower switching means (16) and receives control signals from the low-voltage section (24, 28) exclusively during the duty cycle of the lower switching means (16) as recited in claim 1.

Regarding claim 2: the first circuit section (40, 30, 32, 72) is equipped with at least one first integrating circuit (40, 30, 32, 72) configuration which is charged during

the duty cycle of the lower switching means (16) and discharged during the duty cycle of the upper switching means (14).

Regarding claim 3: the first integrating circuit (40, 30, 32, 72) configuration is equipped with at least one integration capacitor (66) and a charging circuit and a discharging circuit.

Regarding claim 4: elements 64, 62 functions as constant current sources.

Regarding claim 5: a transistor (seen inside 50) provided in the low-voltage section (24, 28) which transmits a signal to the high-voltage section (30, 40, 32, 42, 44) for the duration of the switch-on of the lower switching means (16).

Regarding claim 6: a second circuit section (70, 44, 46) which determines the switch-on instant of the upper switching means (14) as a function of the voltage characteristic of the output voltage (22).

Regarding claim 7: a second circuit section is equipped with a voltage increase recognition circuit with at least one capacitor, one resistor, and one comparator (70).

Regarding claim 8: a second circuit section (70, 44, 46) with means which control the duration of the first dead-time phase before the switch-on of the upper switching means (14) as a function of the duration of the second dead-time phase before the switch-on of the lower switching means (16) by a timer (24) connected to the low-voltage section (24, 28) (because the structure of the claim is fully met so the functional limitation is also met).

Regarding claim 9: the second circuit section (70, 44, 46) is equipped with at least one second integrating circuit configuration which is charged for the duration of the

second dead-time phase, or for the duration of a signal the external timer, and discharged for the duration the first dead-time phase (because the structure of the claim is fully met so the functional limitation is also met)

Regarding claim 10: the structure of the second integrating circuit configuration (70) corresponds to the structure of the first integrating circuit configuration (72).

Regarding claim 11: a voltage decrease recognition circuit with at least one resistor (inherently seen inside 50).

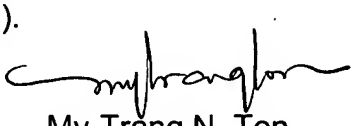
Claim 12 is similarly rejected as claim 1: a driver circuit (Figs. 1-2) for controlling upper and lower switching means (14, 16) for converting a direct voltage (18) into a clocked output voltage (22) for the resonant converter with a high-voltage section (40, 32, 42, 44, 46, 30) for controlling the upper switching means (14) and a low-voltage section (24, 28) for controlling the lower switching means (16) which switch the switching means (14, 16), on alternately, the switch-on phases of the switching means (14, 16) being separated from one another by dead-time phases, characterized by a first circuit section (40, 30, 32), which controls the duty cycle of the upper switching means (14) as a function of the duty cycle of the lower switching means (16) and receives control signals from the low-voltage section (24, 28) exclusively during the duty cycle of the lower switching means (16).

The additional references cited in PTOL 892 to show further analogous prior art circuitry. This art is deemed relevant and should be carefully reviewed before any amendment is filed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

September 21, 2005